## EDITORIAL

We may also be acquainted through my many years of activity in IEEE CPMT and IMAPS (I actually took over as President when ISHM became IMAPS).

While I will be continuing my current consulting business (www.microelectronic-consultants-of-NC.com) and my blog in Solid State Technology, many of you may have seen that last month I accepted the invitation to join forces with Yole Développement (Yole) as a Sr. Technical analyst. I will be using my expertise in the areas of 3D IC, bumping, WLP, IPD, MCMs (SiP) and general thin film processing to contribute to Yole reports, their i-Micronews website and their 3D Packaging magazine (I have been a long time fan of both the website and the magazine).

In this issue, I will be reporting on (1) the recent GSA forum at the Design Automation Conference (DAC) and (2) the Semi/Sematech standards workshop recently held at Semicon West. Singapore startup Doublecheck Semiconductors discusses the carrierless thin wafer handling technology that they have developed with Disco and Fraunhofer IZM, TI's Darvin Edwards discusses their past, present and future in 3D packaging and Randy Kong of DFR Solutions reviews the history of PoP packaging and the quality and reliability issues that were uncovered and resolved.

As a "teaser" for the new Yole report "3D Silicon and Glass Interposers" Jean-Marc Yannou, Jerome Baron and myself share our insights and the thoughts of external technical experts as to what is going on behind the scenes in 3D silicon interposer development.

**Dr Phil Garrou,**
Senior Technical Analyst,
Yole Développement

## EVENTS


- **Electronics System Integration Technology Conference - ESTC,**
September 13 to 16, 2010 - Berlin, Germany

- **Sophia Antipolis forum on MicroElectronics - SAME 2010,**
October 16, 2010 - Sophia Antipolis, France

- **International Wafer-Level Packaging Conference - IWLPC,**
October 11 to 14, 2010 - Santa Clara, CA

## ANALYSIS

# Secrecy shrouds 3D silicon interposer development

**The industry is being extremely secretive at a time when many questions remain unanswered about how technical and supply chain challenges will be handled for 3D silicon interposers.**

Many semiconductor companies—OSATS, CMOS foundries, MEMS foundries, and even organic and glass substrate suppliers—seem to be developing 3D interposers, but aren't officially admitting it yet, says Yole analyst Jérôme Baron. In fact, very few people are willing to talk openly about what they expect to happen with interposers.

For those unfamiliar with the interposer, it's a substrate to which components are attached as an intermediate step prior to direct attachment to a substrate such as a PCB. Through-silicon interposers (TSIs) can be thought of as "carriers" for 3D architectures to accommodate the requirements of ICs with high I/O counts and their high-density routing from the package to the board.

Taiwan Semiconductor Manufacturing Company (Hsinchu, Taiwan) was one of the first to go public about their intentions with silicon interposers, in June 2010, by saying that they're pursuing "multi-die packaging through 2D/3D IC design methodologies, innovative silicon interposer, and through-silicon via (TSV) manufacturing capabilities." That was pretty much the extent of the great revelation. Other companies, such as Taiwan's Advanced Semiconductor Engineering, have made similar announcements that were equally light on details.

image sensors (CIS). Their final intention isn't to package CIS with TSV in France, he says, but rather to find a product to start with, and pull together a team of TSV/WLP-related engineers that can refine a process to later outsource the mass production of the TSVs in their image sensors to Asian subcontractors. The Crolles team will then move on to producing more complex next-gen 3D products such as interposers, TSV in logic, TSV derivative products for the medical and automotive areas, etc.

"We'll likely see many pragmatic industry players follow the same 'holistic' approach," Baron explains. "They all know that 3DIC fully redesigned chips are coming soon, but since no one will get there immediately it's important to first find the right end-product to leverage their 3D TSV/WLP experience. Interposers are the key piece to this pragmatic/holistic approach to full 3DIC integration with TSV."

The question then becomes: Will these interposers be removed in the long run? Baron thinks maybe yes, if it's possible to do it with fully redesigned stacks, but probably not if enough active and functionalities are integrated by then with passive functions, cavities, mature logic functionalities, etc., so that the use of an interposer is justified—even in the long run, when looking at the cost vs. performance tradeoff of using interposers.

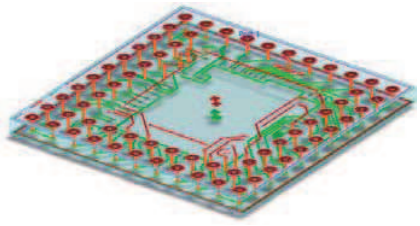
## "Typical applications will be interconnection of a processor and memory with wider bandwidth," explains Seung Wook Yoon, STATS ChipPac

Wondering why silicon interposers seem to be showing up on everyone's radar right now? "It's pretty clear that silicon interposers have the potential to speed the adoption of the first generation of 3D ICs, also known as '2.5D,' without redesigning all of the chip stacking packages in 3D with TSV," Baron explains. "So the most pragmatic players aren't waiting for the availability of fully dedicated tools for 3DIC designs and are jumping on the opportunity to design simple 2.5D ICs based on interposers—to get the first showcase products to market. They can then build upon this experience."

Companies need to begin somewhere, which is what Baron points out STMicroelectronics (Geneva, Switzerland) is doing with its 300mm 3DIC line in Crolles, France, by first producing TSVs for CMOS

### Drivers/Apps

The main application area driving interposer development right now is high-performance computing, according to Eric Beyne, science director of the Advanced Packaging and Interconnect Research Centre (APIC) at Imec (Leuven, Belgium).



*TSV (Courtesy of Ipdia)*

This includes computers, servers, routers, graphic accelerators, FPGA, high-speed optoelectronic transceivers, etc. Also showing potential are RF modules and DC-DC convertor modules where the interposer substrate is also a platform for integrating passive circuit functions (RLC) or simple functions such as ESD protection diodes.

"We see some interest in miniaturization, which seems to be the only real driver today," says Franck Murray, CEO of Ipdia (Caen, France), which is a recent spinout of NXP (The Netherlands) specializing in 3D silicon solutions.

Seung Wook Yoon, in charge of technology marketing of next-gen integration technology at STATS ChipPAC (Singapore), believes that typical applications will be interconnection of a processor and memory with wider bandwidth applications to meet increased electrical performance requirements in advanced semiconductor nodes less than 40nm. "Once TSV technology reaches a mature stage, it will be useful for 3D heterogeneous integration," he adds.

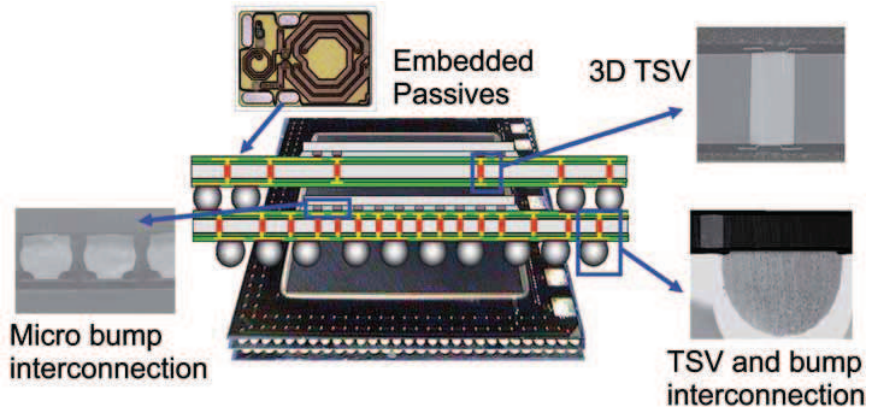
as some MEMS/IC stacking. And the main driver for that application is a trial for improving wafer yield by partitioning/stacking multiple devices. "When both devices are in a single die with a SOC design, yield loss is generally regarded as the biggest problem," he says.

Another perspective, offered from an anonymous source (in keeping with the whole secrecy theme, which is actually an effort to protect intellectual property), is that the performance limitation and cost of organic substrates are behind the drive to adopt the silicon technology.

## Benefits of silicon interposers

One of the primary benefits of using 3D interposers is reducing the gap between the silicon IC and organic substrate. This is followed closely by improving electrical performance and dropping the cost of the system.

A benefit Murray points out is miniaturization when compared to laminates, in the form of smaller pitches and a reduced thickness. There's also a




*TSV silicon Interposer schematic for PoP applications (Courtesy of STATS ChipPac)*

It's important to have a bridge technology for 3D TSV. "A 3D interposer is a great off-chip interconnection component for extreme-low-k (ELK) devices and high-performance applications," Yoon explains. "TSV interposers also have the potential to replace advanced substrates due to advantages in thermal performance, precise dimension control, fine line width/spacing, embedded passives, as well as overall thickness. For this reason, the cost/performance crossover between silicon interposers and advanced substrates is expected to occur in the near future."

performance improvement when combined with integrated passives, he notes.
Yoon believes that 3D interposers offer superior electrical performance, high-density system integration with fine pitch and line width, wafer-level and batch process, absence of thermal expansion mismatch (so micro flip chip interconnection and Cu/ELK/ULK interconnects are possible), thin film process for embedded passives, excellent thermal conductivity of silicon, and heterogeneous integration with CMOS, RF, MEMS, and WLCSP process.

**"Flexibility in device design and supply chain are also key benefits of TSI," Bioh Kim, EV Group, concurs**

Bioh Kim, global business development manager at EV Group (St. Florian, Austria), reports that the main application he's seeing so far for silicon interposers is memory and logic stacking, as well

Beyne views the ability to split digital and analog interface circuits in two chips as being a key benefit because each can follow a different cycle and technology node (faster access to leading nodes for digital). Another benefit he sees is integrating memory or memory stacks close to processor units with short, high bandwidth (many I/O) interconnects, avoiding the use of vertical stacking DRAM on high-power ICs. And yet another benefit is the integration of capacitive decoupling and other passive functions (possibly also supporting simple circuits such as ESD protection).

"Flexibility in device design and supply chain are also key benefits," Kim concurs. "Any devices can be integrated without limits."

## Materials

Which will it be: Silicon wafer, silicon panels, glass, or LCD glass panels? All of these materials are under consideration for 3D interposers. Oddly enough, some consensus can be found here.

Nearly everyone says the material of choice is silicon wafers, preferably 300mm. "Silicon will be a major material for 3D TSV interposers because TSV can adopt silicon process technologies with available equipment and materials suppliers, and electrical designs on silicon are well understood," Yoon says. Glass, however, may be available for other applications, including MEMS, CIS, RF, MOEMS or optical ones.

Kim believes that silicon and glass will be the most dominant. "Cost-wise, even polycrystalline silicon can be used because it isn't a real functional layer. Georgia Tech's Microsystems Packaging Research Center (Atlanta, Georgia) started a consortium to adopt large glass panels, but an issue is whether all related equipment suppliers can provide related tools handling large substrates," he adds.

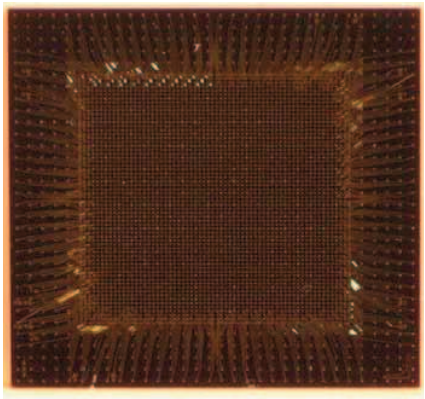
An anonymous source closely involved with substrates offers a different opinion, suggesting that combining the wafer process, panel process, and LCD processes will offer the greatest potential for cost reductions.

## Mask aligners vs. steppers

Will TSI/silicon interposers be patterned using mask aligners or steppers? Still no real consensus to be found on this issue, except that both can be used and it will likely depend in large part on the application and density requirement.

Yoon, for example, expects to see both used, based on application and adopted technology. For high-density interconnect applications, he thinks steppers are a good option, but points out that an aligner can also be used for RDL or other processes based on the design rule or dimension.

Beyne thinks steppers will be used, citing overlay accuracy requirements and line width and spacing requirements.
And Kim says patterning with a mask aligner is likely, because RDL and TSV will be necessary in many applications. He notes that steppers can be used, but he thinks mask aligners are suitable for applications like WLP.



*3D silicon interposer (Courtesy of Allvia)*

## Routing layers

How many routing layers can be on the front/back? Again, no solid consensus here.

The minimum necessary to reduce costs ranges from one up to five, according to Beyne. "One or two interconnect routing layers, with two layers for power and ground distribution. There will only be routing on the front side because the backside is only bumps on TSV," he says.

Murray weighs in with "two to three" layers.

"It depends on routing complexity, but based on industry studies and current work within STATSChipPAC, we believe two layers on front and one on the back will be good enough for most of interposer applications," says Yoon.

"Multiple layers of Cu/polymer can be deposited on the front side, where vias are etched for TSV formation, especially if embedded structures or multiple BEOL layers are needed," Kim says.

## Other technical challenges

There are other technical challenges that need to be resolved for silicon interposers. Yoon says these include: the codesign ecosystem (device design and fabrication, packaging, and testing) and industrial standards; a thin wafer handling system (300mm), temporary bonding/debonding process, process temperature, as well as new materials sets; a packaging solution for TSV, and a need to prove TSV/microbump reliability after packaging; test methodology, wafer-level or die-level TSV test and package-level test, inline TSV test approach; and a 3D TSV failure analysis technique because new techniques are needed to isolate and identify TSV failure modes clearly.

Kim reports that he's seeing lots of concern about thin interposer handling during stacking devices on both sides, that the main question is carrier transfer from one side of the interposer to another side during stacking devices on each side.

And Beyne is concerned about design tool readiness for silicon interposers.

## Cost

Shifting over to the business end of things, cost is still a key hurdle slowing the adoption of silicon interposers for 3D.

This is a huge issue compared to laminates or any other PCB-like competing solution, according to Murray. "It's not realistic to think that etched glass or silicon can reach the same prices," he says.

The cost of 3D interposers hasn't been fully explored according to Yoon, but he thinks it delivers a unique advantage in applications that combine performance and form factor in a very competitive cost. "To further widen applications that are more cost sensitive, integrating additional devices such as integrated passive devices on the interposer can be considered," he adds.

"Yes, cost is still an issue, but it's application dependent. High-volume manufacturing is required to reduce cost, due to the high capital investment for such a fab. Use of old fabs running a 'fat' metal BEOL seems a good initial starting point, limiting the investment to 3D TSV technology," notes Beyne.

"Many companies are considering using silicon interposers for their main IC business," Kim says. "One way to drop the cost is to go with low-cost substrates like large glass or polycrystalline silicon, although I'm not sure whether the big IC suppliers will like that."

## Supply chain challenges

One of the biggest issues for silicon interposers today, Murray asserts, is that there isn't a supply chain in place. And accordingly, Beyne wants to know who will supply the interposers. Will it be foundries, SATS, or package substrate suppliers?

Yoon expects to see a business model for 3D interposers quite similar to those currently seen for organic substrates or leadframes. "There should be one party to provide TSV interposers, including testing. STATS ChipPAC envisions providing a turnkey solution with 3D TSV interposers. The supply chain challenge is there mainly due to the lack of an industrial standard of footprint and interconnect methods," he says.

"If using silicon interposers, we can have more flexibility in the overall supply chain for devices like memory and logic. The only issue is who will provide patterned interposers with RDL and TSV," says Kim. "I assume it is a good business for foundry companies."

**"Use of old fabs running a 'fat' metal BEOL seems a good initial starting point," explains Eric Beyne, APIC**

## Timeline

It appears that the first applications will be coming soon: In the 2012-2013 range, with high-performance applications and mixed-signal leading the way. Mostly everyone agrees upon that.

An anonymous source expects that for logic and memory stack, product will come within two years. But for CPU and full 3D stacked with interposer, it's unclear if that'll happen within five years—based on current technology and industrial status. This may change with time and technology innovation.

And definitely worth noting, Kim cautions that if additional cost and form factors aren't leveraged enough, compared to performance improvement, people will look for a way to eliminate interposers. In fact, he's already seeing some signs of people trying to avoid using interposers altogether.

**Sally Cole Johnson for Yole Développement**

**Jérôme Baron** leads Yole's MEMS and Advanced Packaging market research. He has been involved in the technology analysis of the 3D packaging market evolution at device, equipment, and material supplier levels. Baron earned a MSc. Degree in Micro and Nanotechnologies from the National Institute of Applied Sciences in Lyon, France.

**Eric Beyne** is scientific director of the Advanced Packaging and Interconnect Research Centre (APIC) at Imec. He obtained a degree in electrical engineering in 1983 and a Ph.D. in applied sciences in 1990, both from the University of Leuven. He has been with Imec since 1986 and is president of the IMAPS-Benelux committee, member of the IMAPS-Europe Liaison committee, elected member of the board of governors of the IEEE-CPMT society and IEEE-CPMT strategic director for Region 8.

**Bioh Kim** manages global business development at EV Group, primarily for semiconductor packaging, 3D integration, and thin wafer handling. Prior to joining EVG, Kim worked at Samsung Electromechanics, Semitool, and Cookson Electronics (Enthone).

**Franck Murray** is IPDIA's CEO. He has more than 25 years' experience working in the semiconductor industry. A graduate of L'Ecole Centrale de Paris, he was most recently the director of technology for NXP Semiconductors France.

**Seung Wook Yoon,** Ph.D., MBA, is in charge of technology marketing of next-generation integration technology at STATS ChipPAC, including TSVs, embedded packaging, integrated passive device, and 3-D IC packaging. Prior to joining STATS ChipPAC, he was deputy lab director of the Microsystem, Module, and Components Lab at the Institute of Microelectronics in Singapore. Yoon received a Ph.D. in materials science and engineering in 1998 from KAIST in Korea. He also holds a MBA from Nanyang Business School in Singapore.